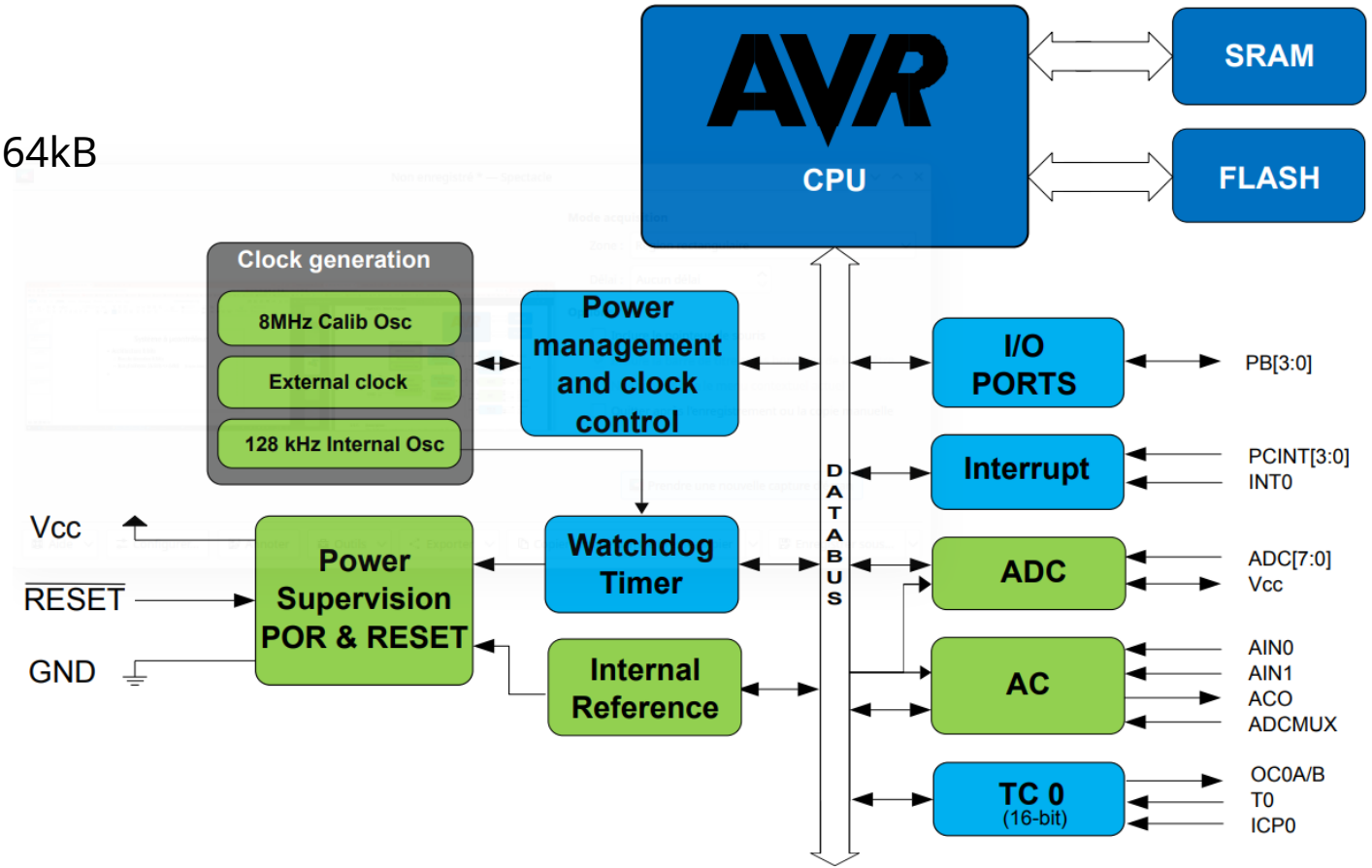
Systèmes embarqués

- Choix architecture matérielle
- Bare Metal / OS
- Consommation énergie
- Temps réel
- Partage de ressources
- Application à l’iot

Système à µcontrôleur

- Architecture 8 bits
  - Bus de données 8 bits
  - Bus d'adresse 16 bits => 64kB
    (B:byte, b:bit)
- Harvard architecture
  - Vs « von Neumann »
  - Bus données
  - Bus instructions
  - Plus complexe
- RISC Architecture
  - Vs CISC



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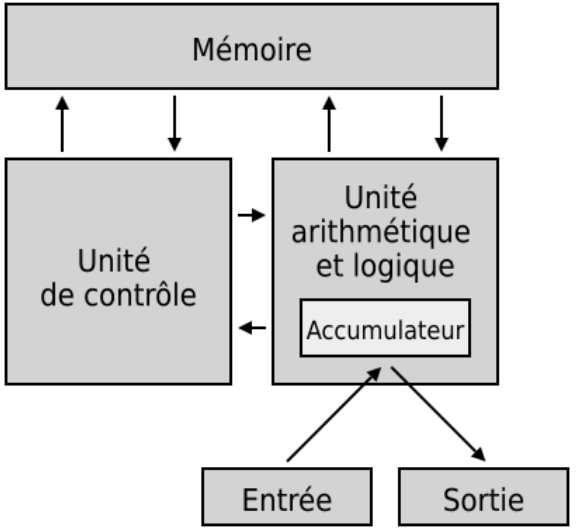

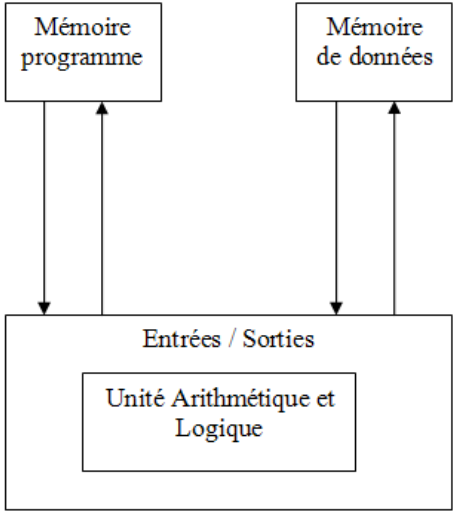

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CISC	RISC
The original microprocessor ISA	Redesigned ISA that emerged in the early 1980s
Instructions can take several clock cycles	Single-cycle instructions
Hardware-centric design – the ISA does as much as possible using hardware circuitry	Software-centric design – High-level compilers take on most of the burden of coding many software steps from the programmer
More efficient use of RAM than RISC	Heavy use of RAM (can cause bottlenecks if RAM is limited)
Complex and variable length instructions	Simple, standardized instructions
May support microcode (micro-programming where instructions are treated like small programs)	Only one layer of instructions
Large number of instructions	Small number of fixed-length instructions
Compound addressing modes	Limited addressing modes

Support attiny841 : utilisation d’eclipse

- https://fr.wikipedia.org/wiki/Jeu_d'instructions
- https://ww1.microchip.com/downloads/en/DeviceDoc/Atmel-8495-8-bit-AVR-Microcontrollers-ATtiny441-ATtiny841_Datasheet.pdf
- Liste des registres
- Fichier elf/lss
- Interrupt Vectors

Support attiny841 : consommation

- Consommation statique
  - Tension d’alimentation
- Consommation dynamique
  - Fréquence
- Sleep Modes
- Impact sur les performances