

FABRICATION DES CIRCUITS IMPRIMES

V Gammes de fabrication

PRINTED CIRCUIT BOARD FABRICATION

V Operation Flow

Gammes de Fabrication

Operation Flows

- | | | |
|----------|-----------------------------|----------------------------------|
| 1 | Circuit simple face | <i>Single-sided board</i> |
| 2 | Circuit double face | <i>Double-sided board</i> |
| 3 | Circuit multicouches | <i>Multilayer board</i> |
| 4 | Circuit souple | <i>Flexible board</i> |
| 5 | Circuit Flexo-rigide | <i>Flex-rigid circuit</i> |

1

Circuits Simple Face Principe de base

Single-Sided Board *Overview*

Sommaire

Outlook

- Diagramme
- Vue côté soudure
- Matière de base
- Transfert image
- Gravure
- Élimination de la
résine photosensible
- Perçage

Flow-chart

Solder-side view

Base material

Imaging

Etching

Stripping

Drilling

Sommaire

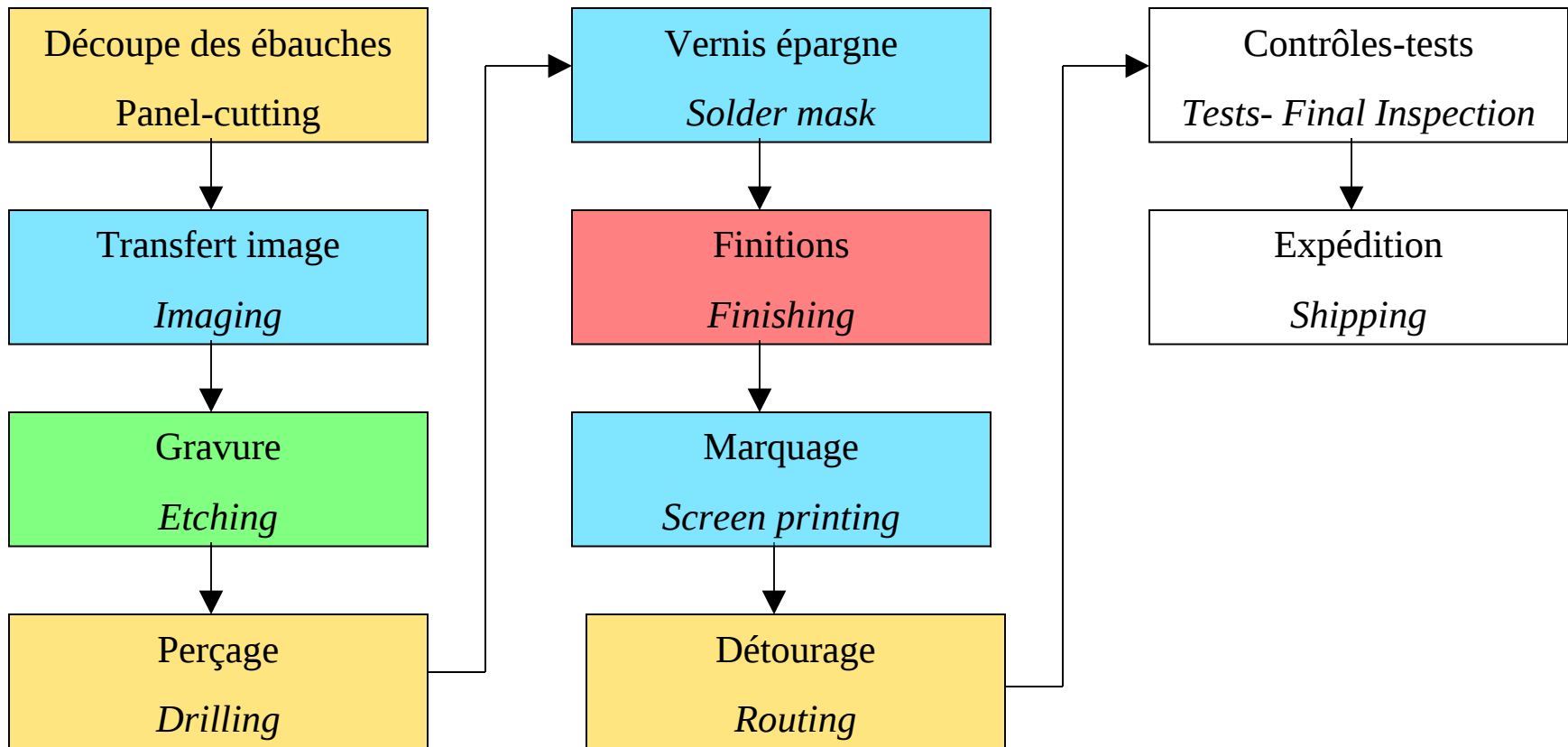
Outline

- Vernis épargne-soudure
- Traitement du cuivre
- Marquage
- Détourage
- Test électrique
- Contrôle
- Expédition

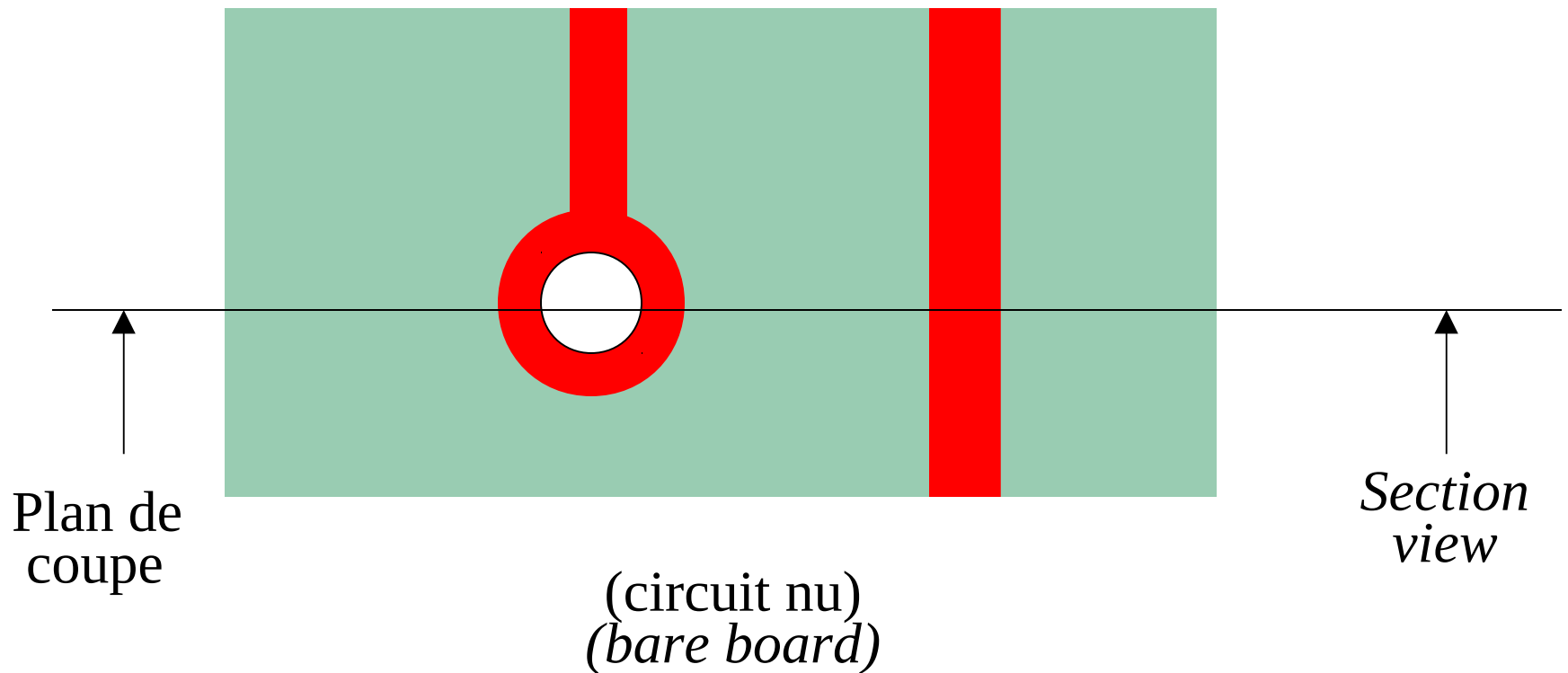
Solder mask
Copper-finishing
Screen-printing
Routing
Electrical test
Inspection
Shipping

Diagramme

Flow chart



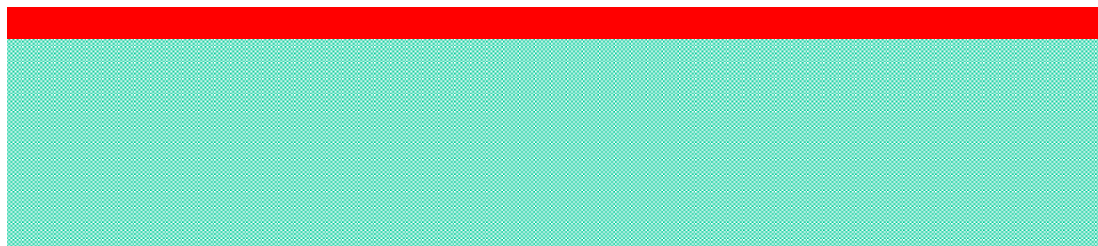
Vue côté soudure *Solder side view*



Matière de base

Base Material

Cuivre 9 à 105 μm
9 to 105 μm copper



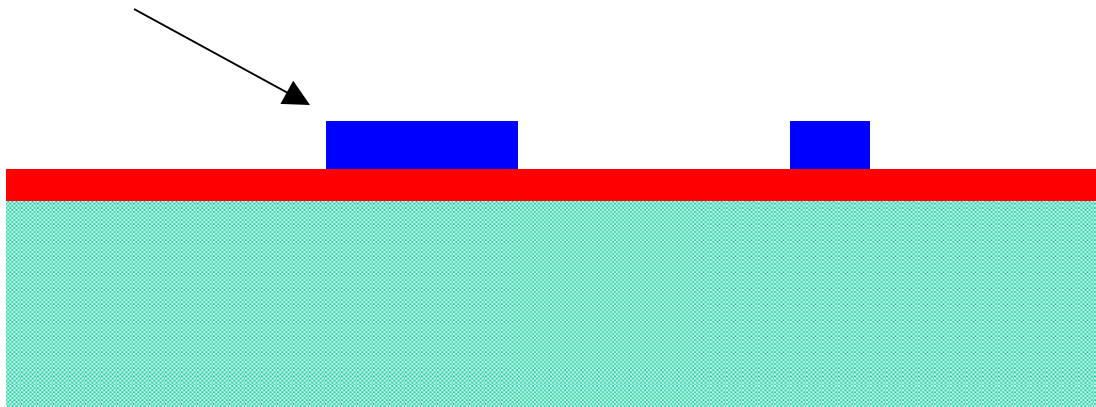
Stratifié 1 à 3,2 mm (FR2, FR3, FR4, CEM)
1 to 3.2 mm laminate (FR2, FR3, FR4, CEM)

Transfert image

Imaging

Réserve de gravure : encre
ou résine photosensible

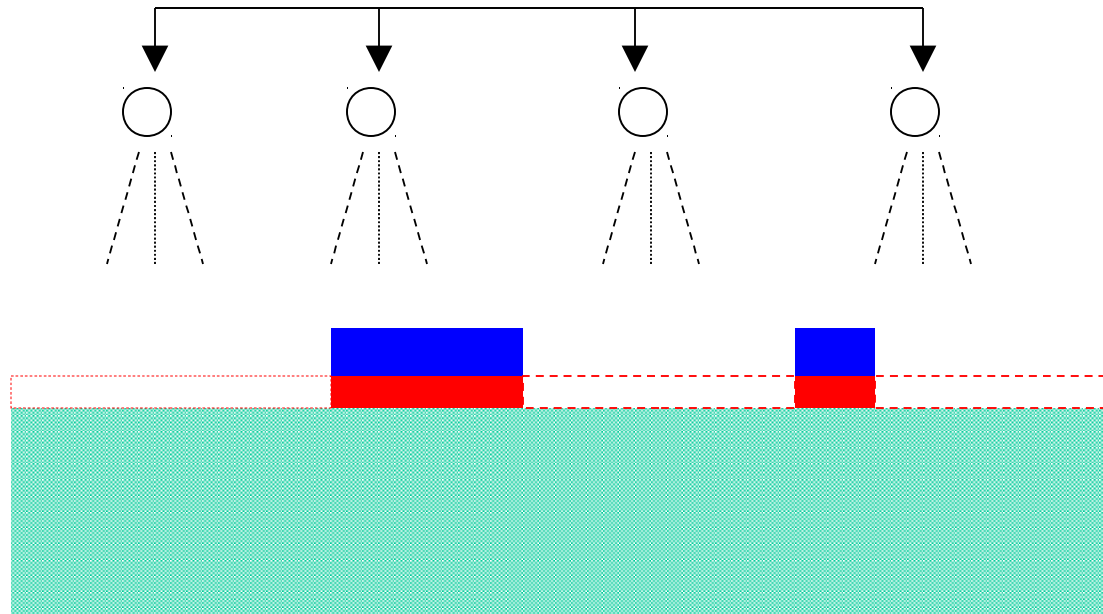
*Etch mask : ink or
photoresist*



Gravure

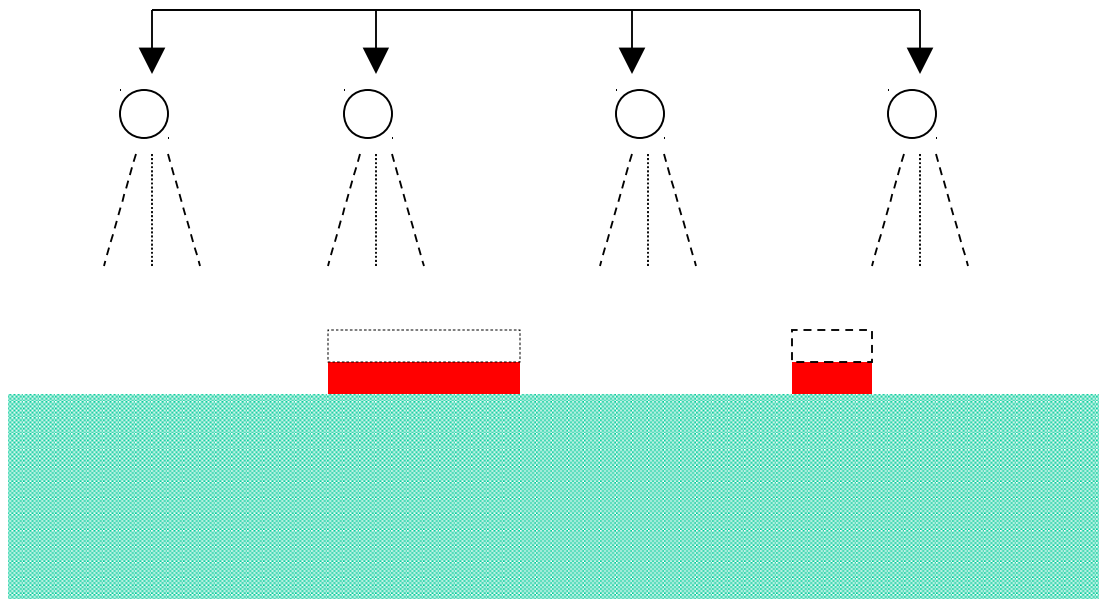
Etching

Pulvérisation de l'agent de gravure
etchant spray

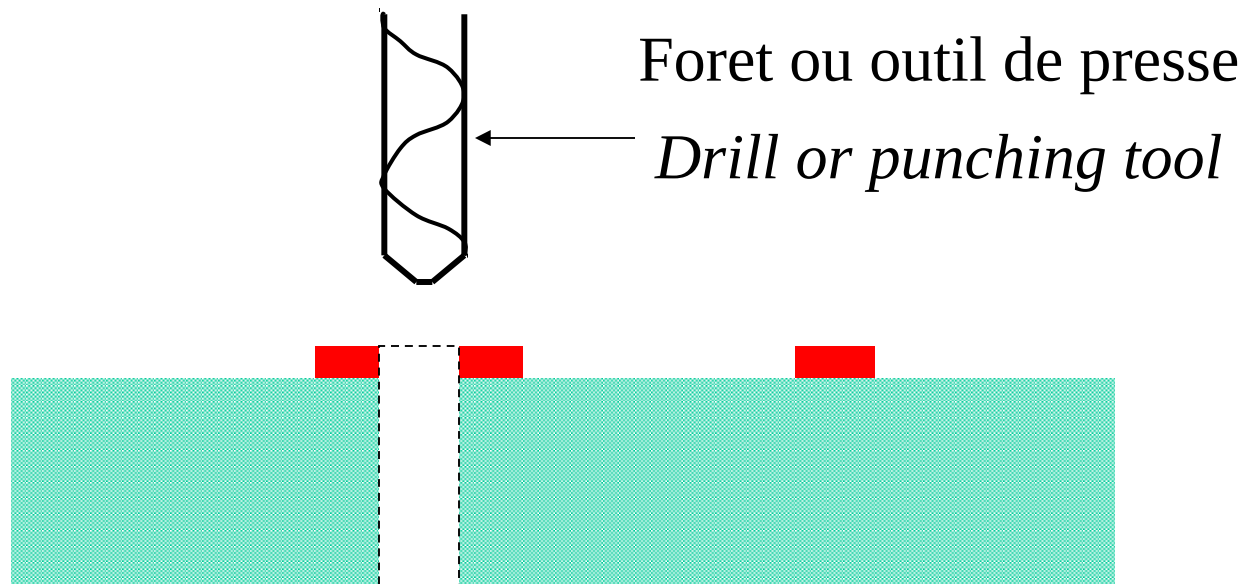


Élimination de la réserve de gravure *Stripping*

Pulvérisation de solvant
stripper spray

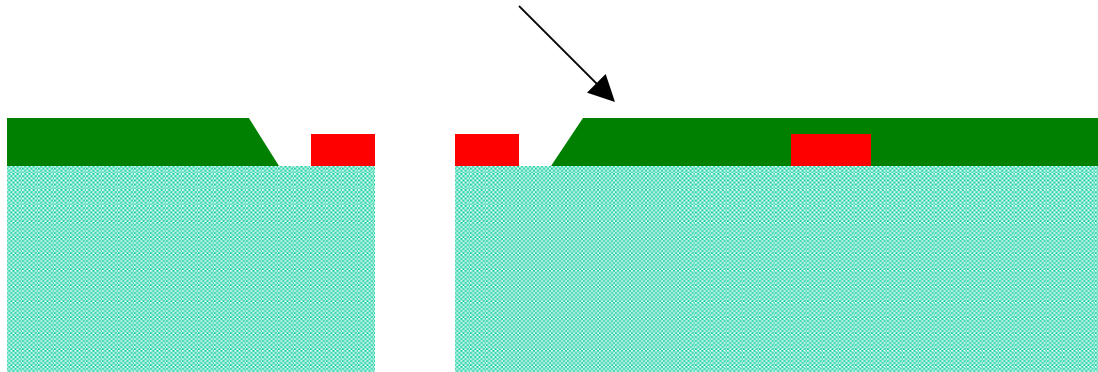


Perçage / Poinçonnage *Drilling / Punching*



Vernis épargne-soudure *Solder mask*

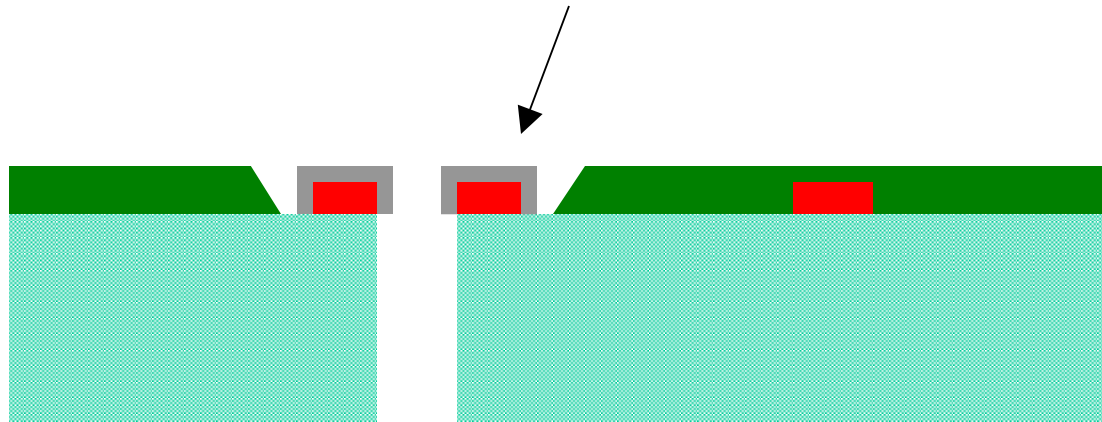
Dépôt de vernis par sérigraphie
Screen-deposited solder resist



Traitement du cuivre

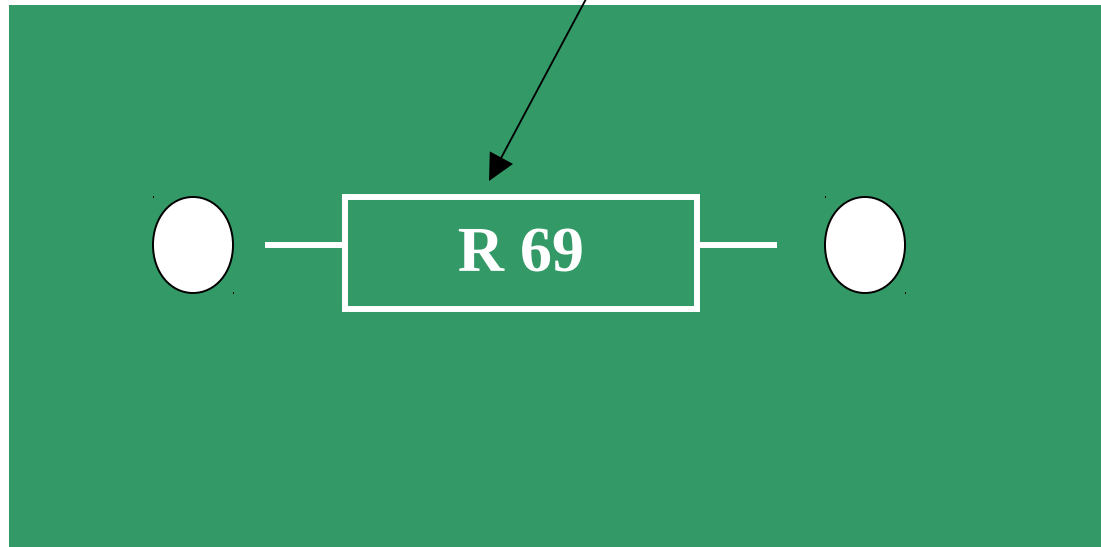
Copper finishing

étamage / passivation
tinning / passivation



Marquage *Screen printing*

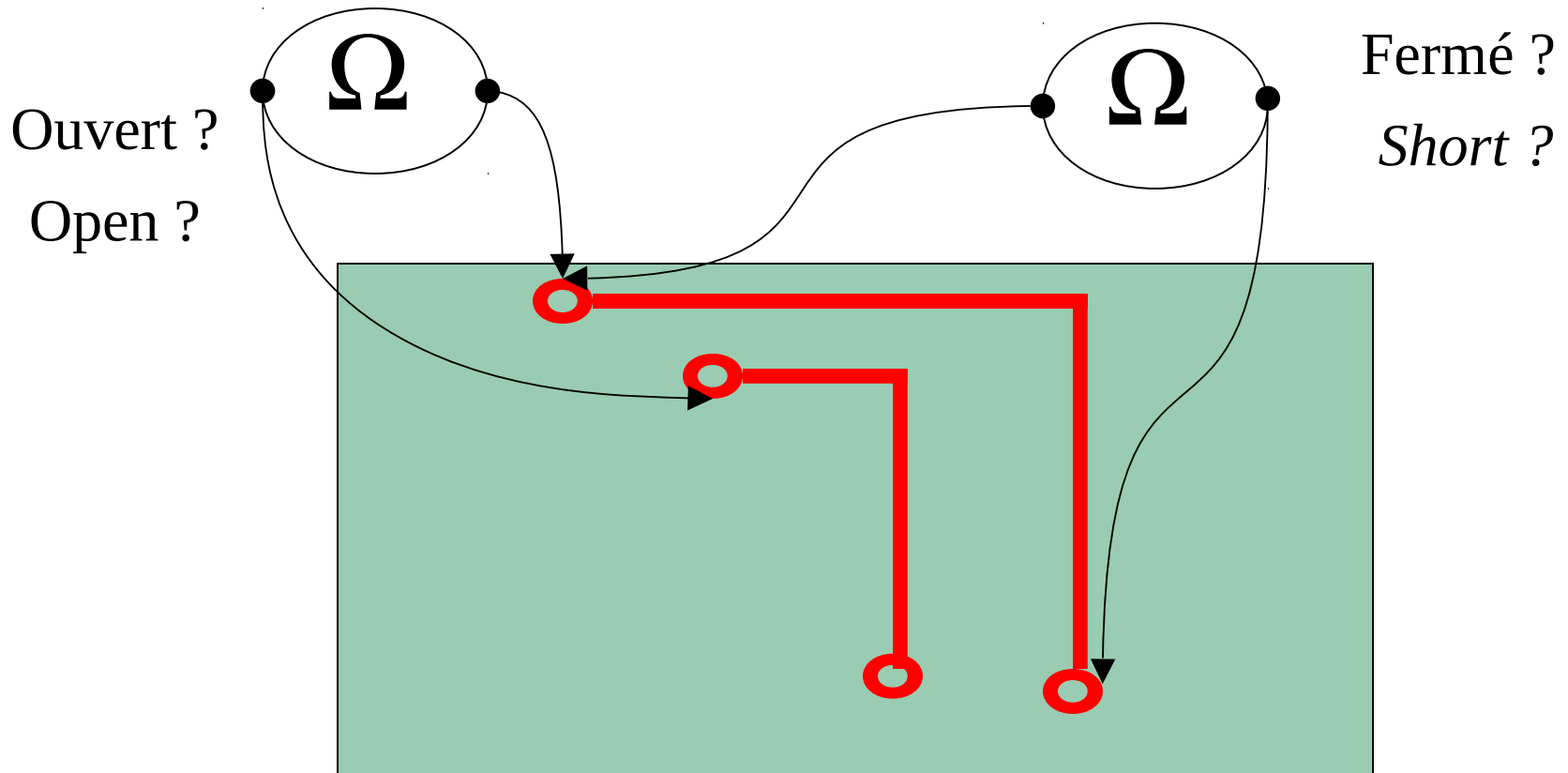
Sérigraphie du motif
screen-printing



Côté composants
component layer

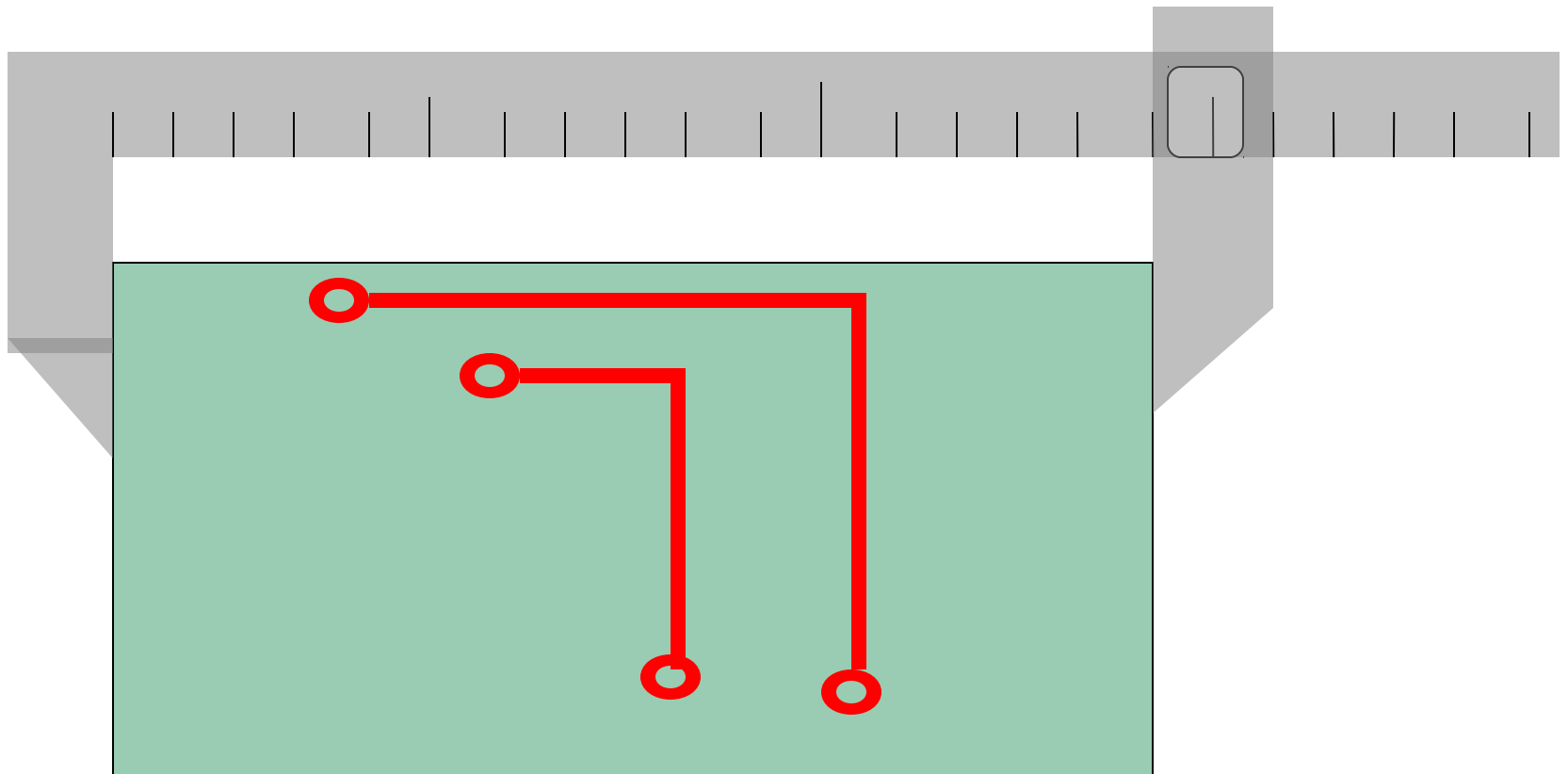
Test électrique

Electrical test



Contrôle

Final Inspection



Expédition *Shipping*



2

Circuits Double Faces Trous Métallisés Principe de base

Double-Sided Plated-Through Hole Boards *Overview*

Sommaire

Outlook

- diagramme
- Vue côté composant
- Matière de base
- Perçage
- 1ère métallisation
- Transfert image
- 2ème métallisation
- Élimination de la résine

Flow-chart

Component side view

Base material

Drilling

1st plating

Imaging

2nd plating

Photoresist stripping

Sommaire *Outline*

-Gravure	<i>Etching</i>
-élimination SnPB	<i>SnPb stripping</i>
-Vernis épargne-soudure	<i>Solder mask</i>
-Étamage H.A.L.	<i>H.A.L. tinning</i>
-Marquage	<i>Screen printing</i>
-Détourage	<i>Routing</i>
-Test électrique	<i>Electrical test</i>
-Contrôle	<i>Inspection</i>
-Expédition	<i>Shipping</i>

Diagramme *Flow-chart*

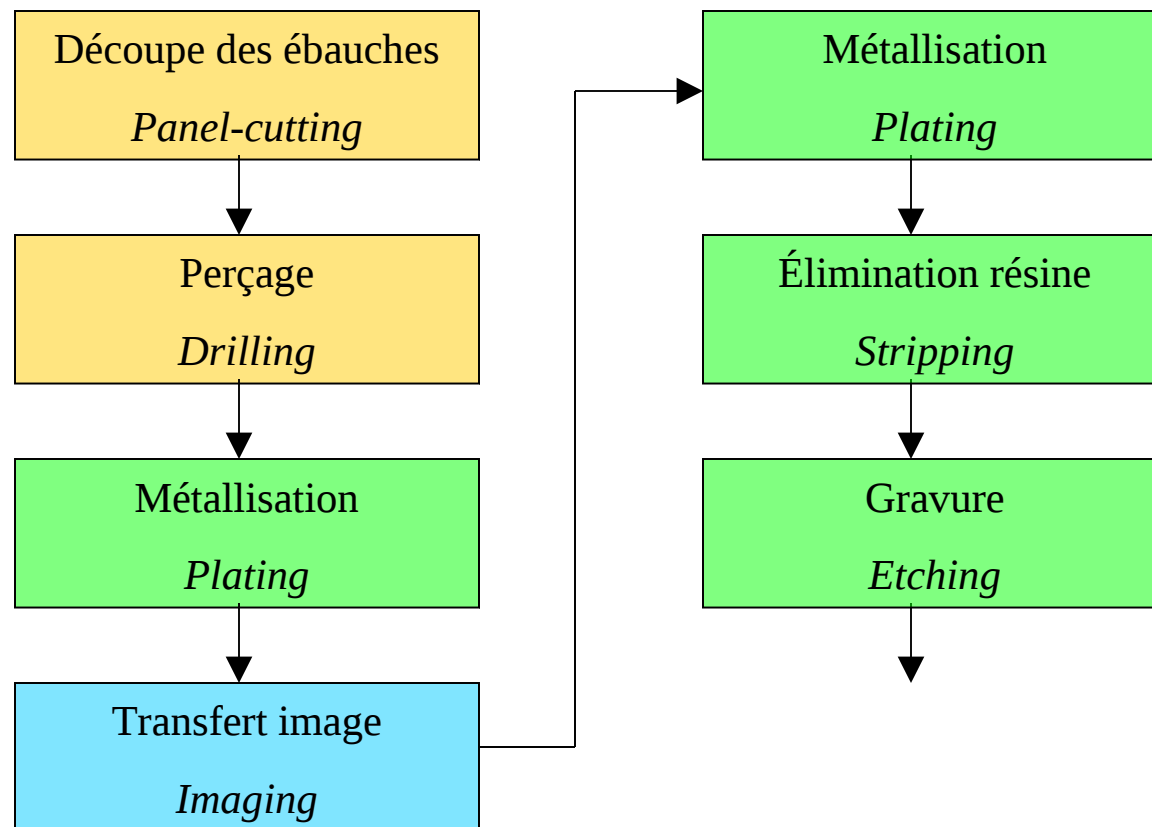
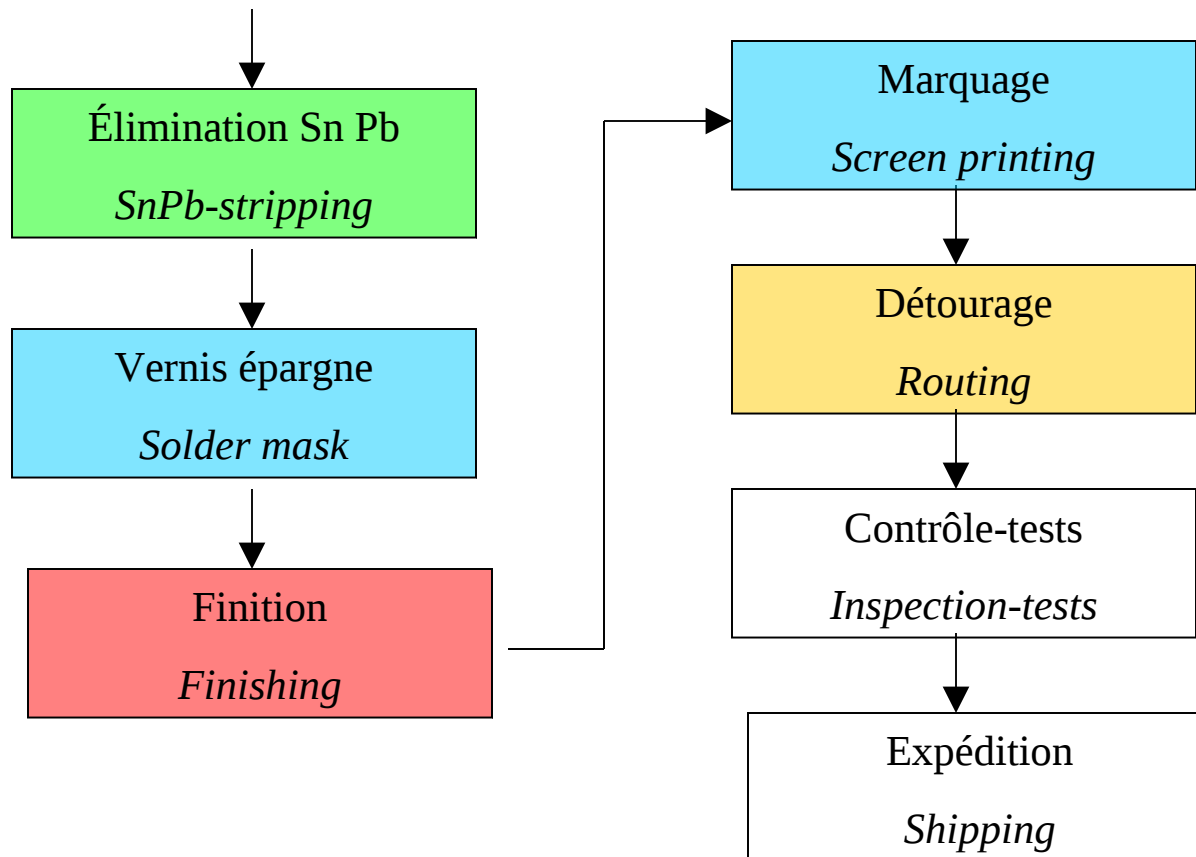
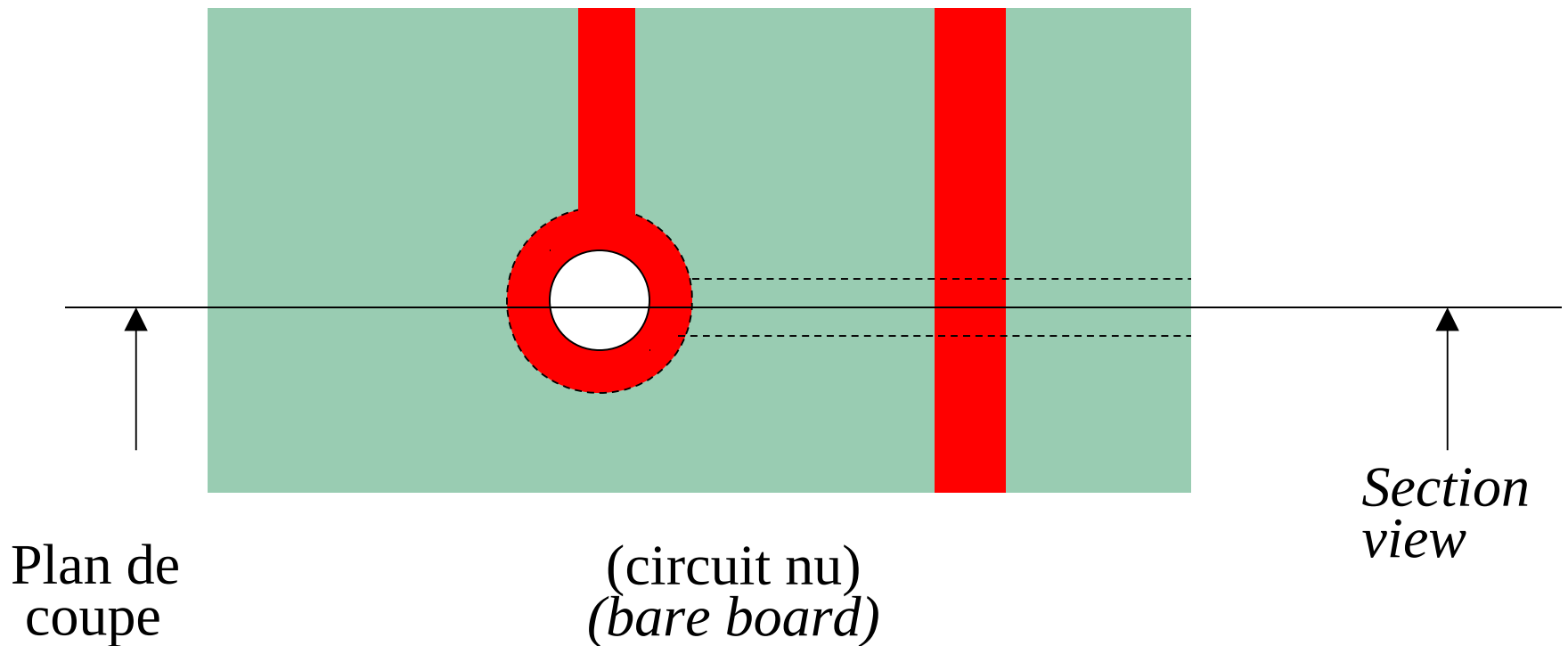


Diagramme *Flow-chart*

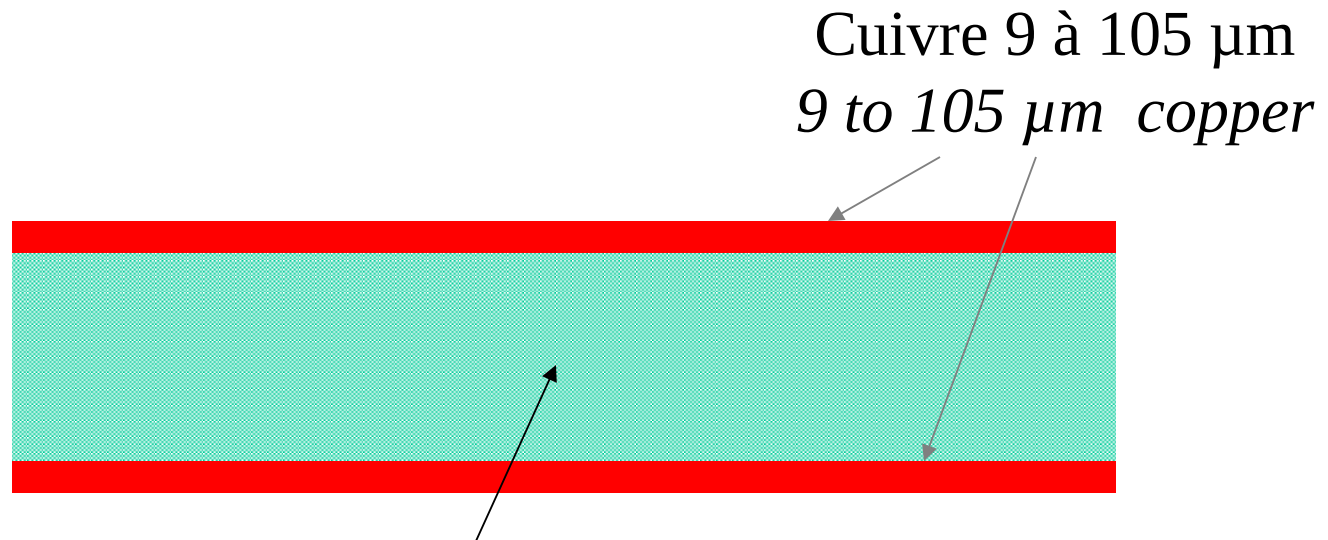


Vue côté composants *Component-side View*



Matière de base

Base material

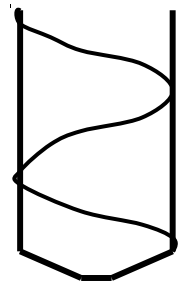


Cuivre 9 à 105 μm
9 to 105 μm copper

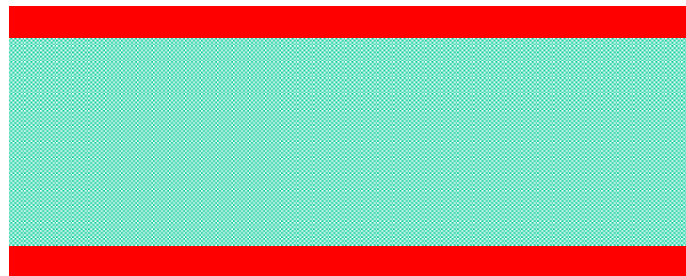
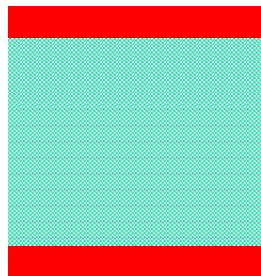
Stratifié 1 à 3,2 mm (FR4, CEM3)
1 to 3.2 mm laminate (FR4, CEM3)

Perçage

Drilling



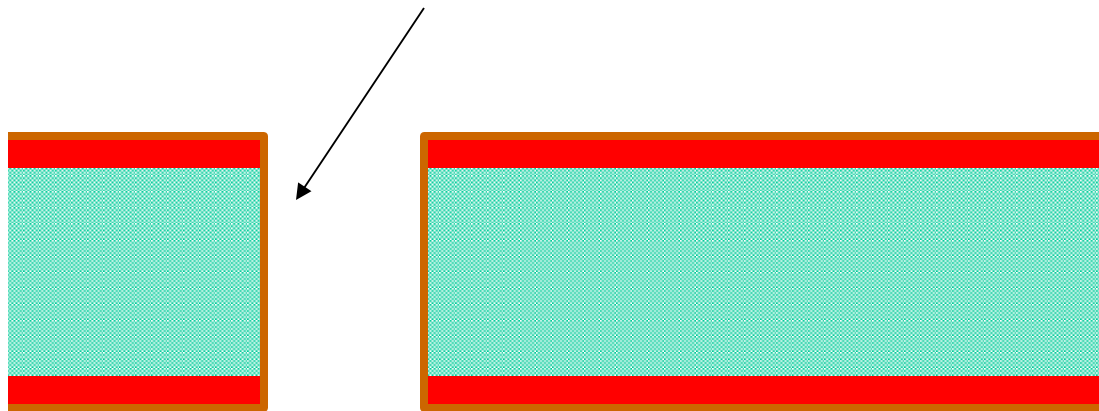
foret
drill bit



Première métallisation

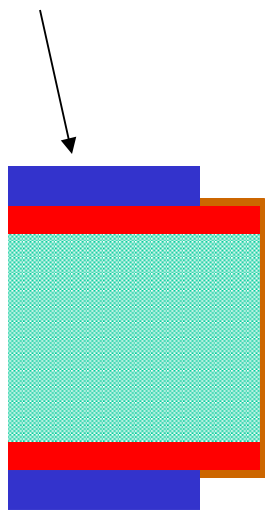
First plating

Cuivre chimique + renfort électrolytique
electroless copper + electrolytic copper plating

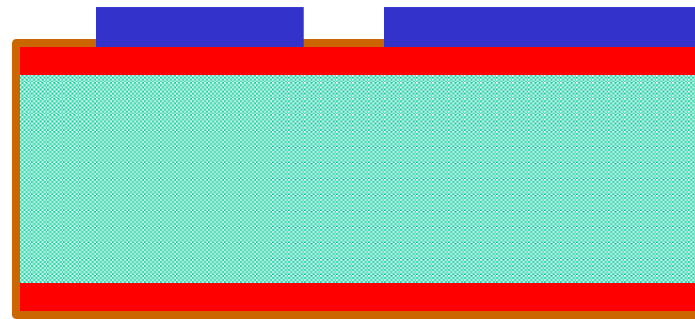


Transfert image *Imaging*

Réserve de métallisation
(résine photosensible)



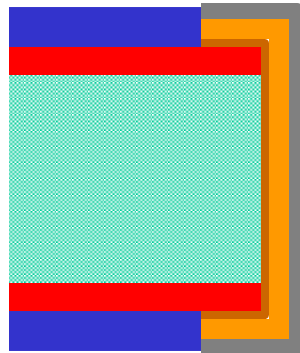
Plating mask
(photoresist)



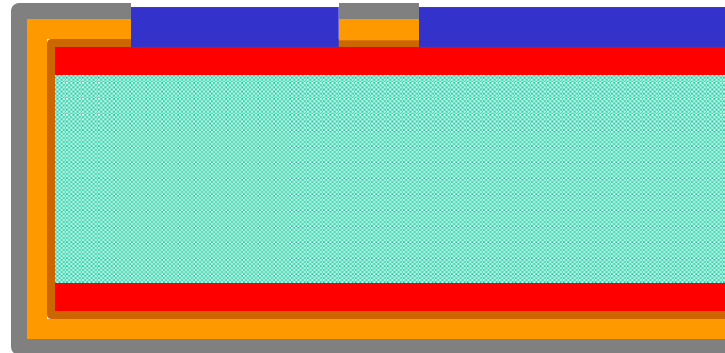
Seconde métallisation

Second plating

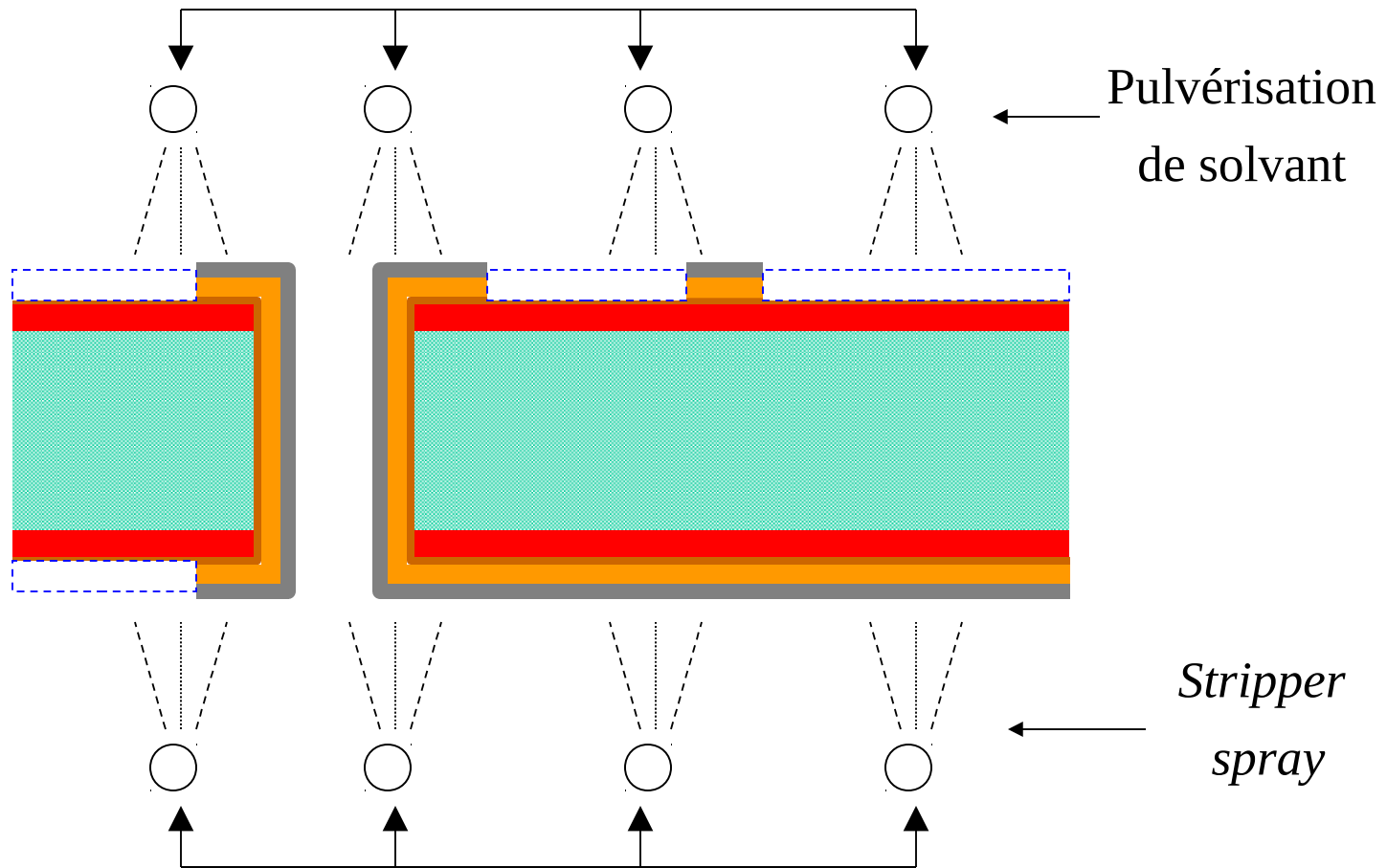
Dépôt électrolytique de cuivre (25 μm) et alliage (5 μm)



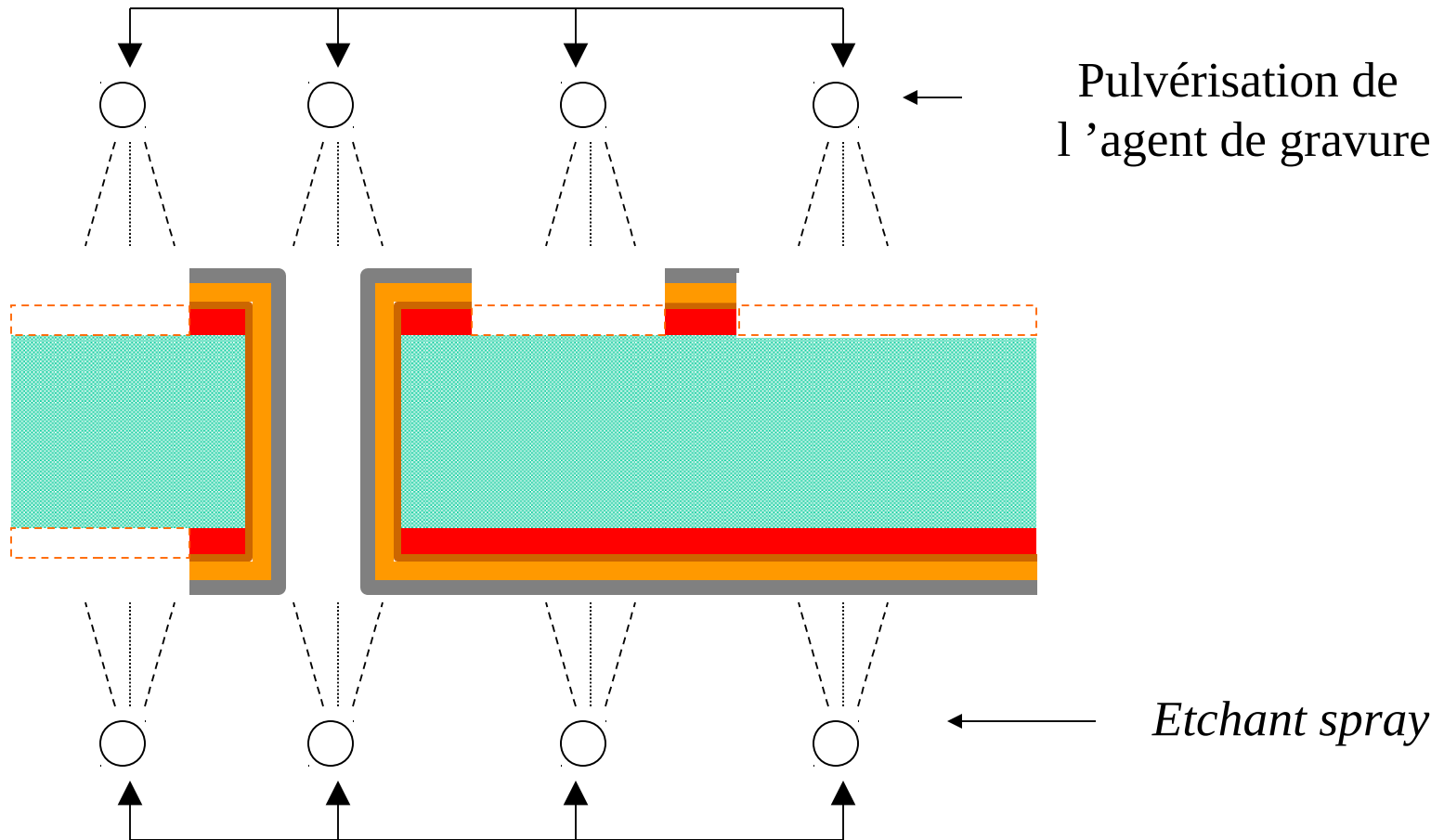
*Copper plating (25 μm)
+ alloy plating (5 μm)*



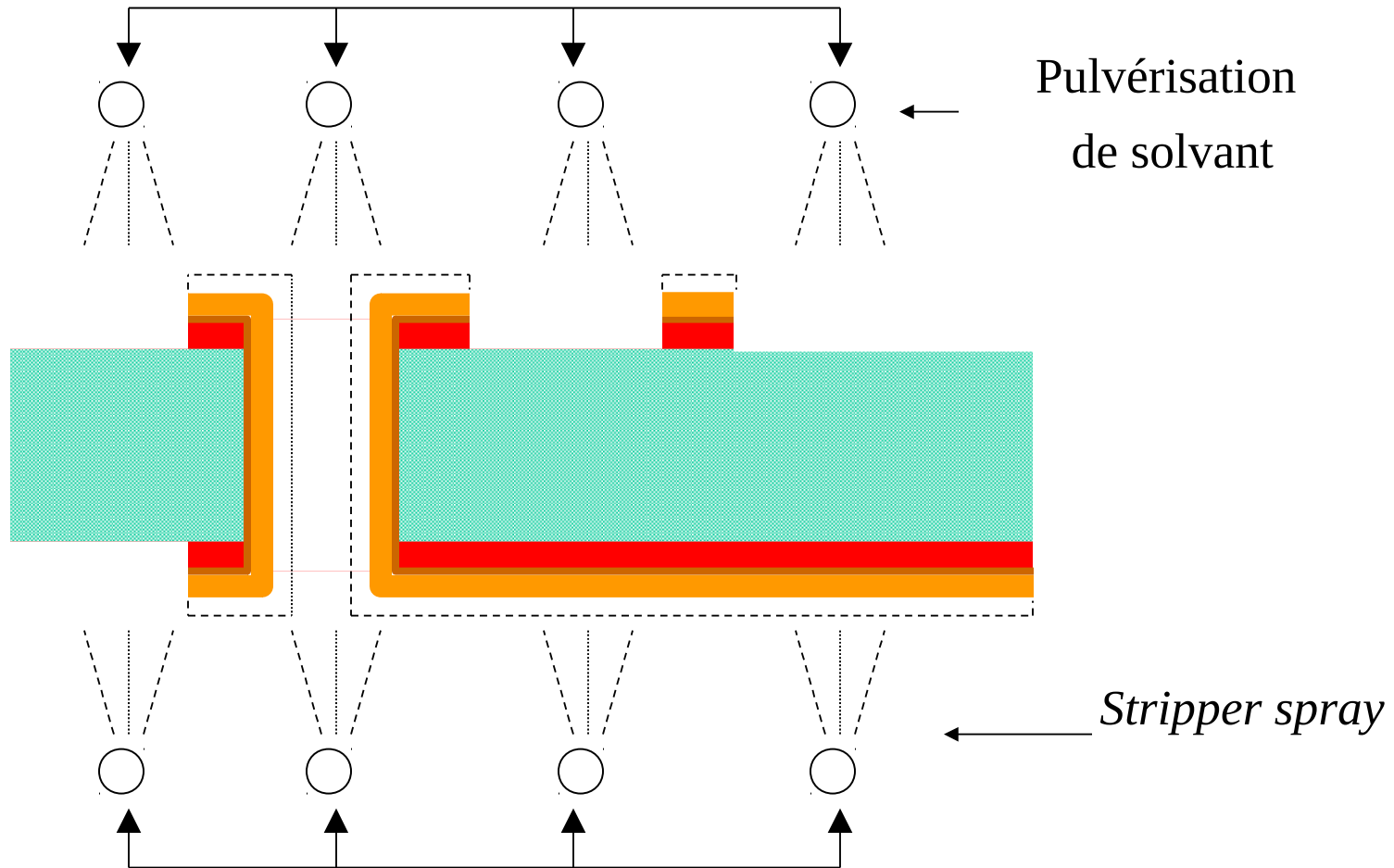
Elimination de la réserve *Stripping*



Gravure *Etching*

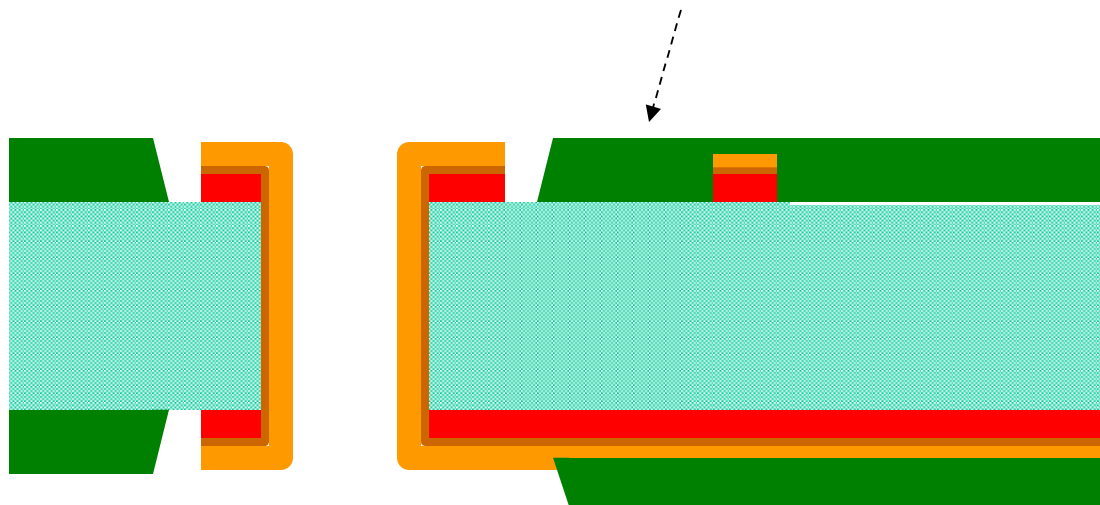


Elimination du dépôt SnPb *Stipping*



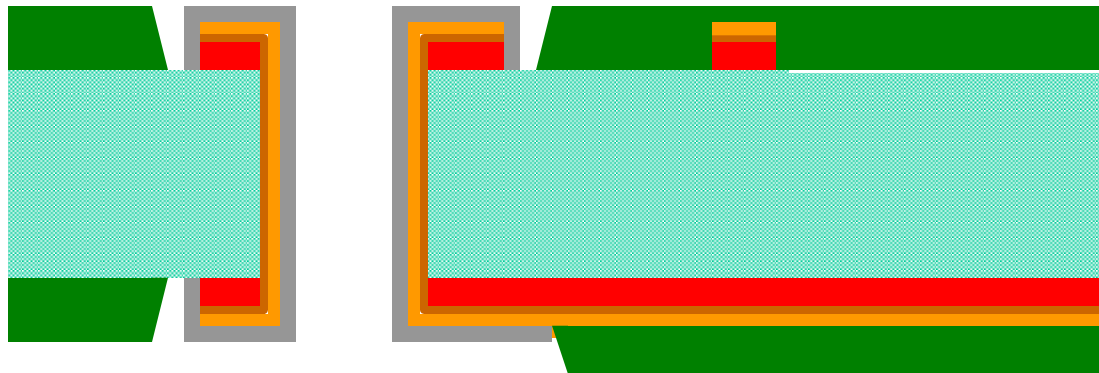
Vernis épargne-soudure *Solder mask*

Dépôt de vernis par sérigraphie
Screen-deposited solder resist



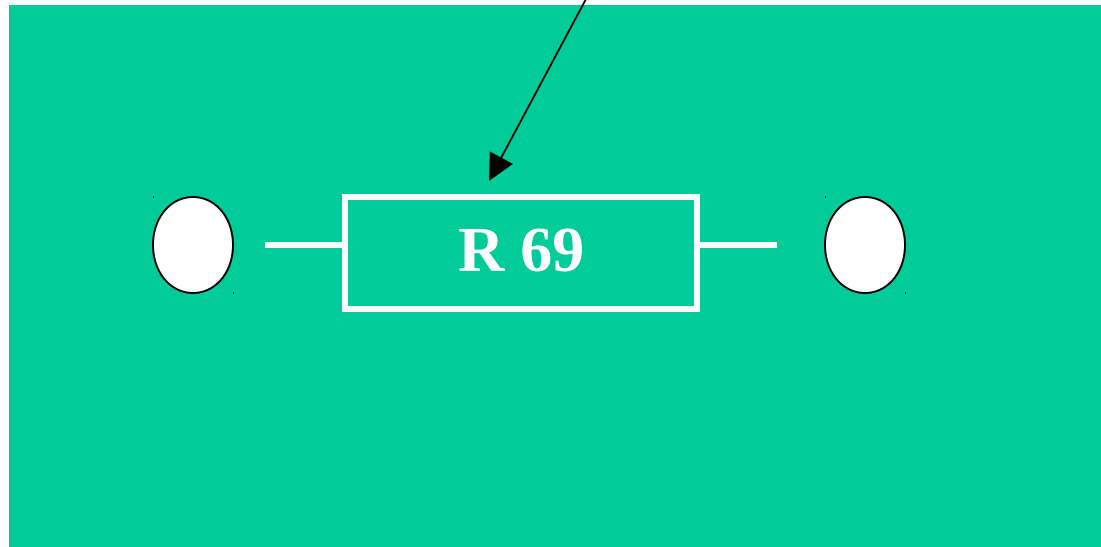
Etamage H.A.L. *H.A.L. tinning*

Dépôt SnPb par bain et nivelage à l'air chaud
Tin bath deposit and hot air levelling



Marquage *Screen printing*

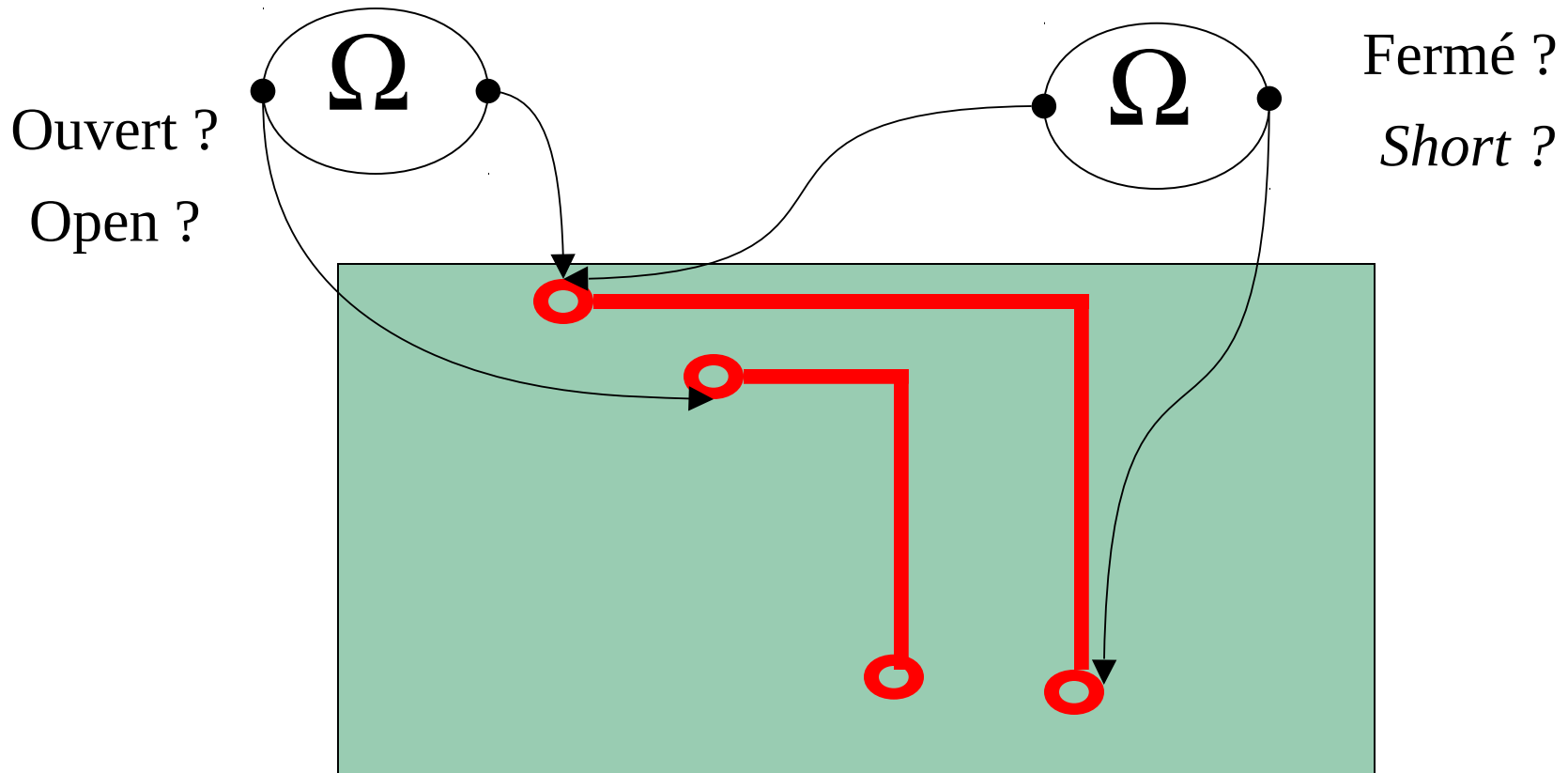
Sérigraphie du motif
screen printing



Côté composants
component layer

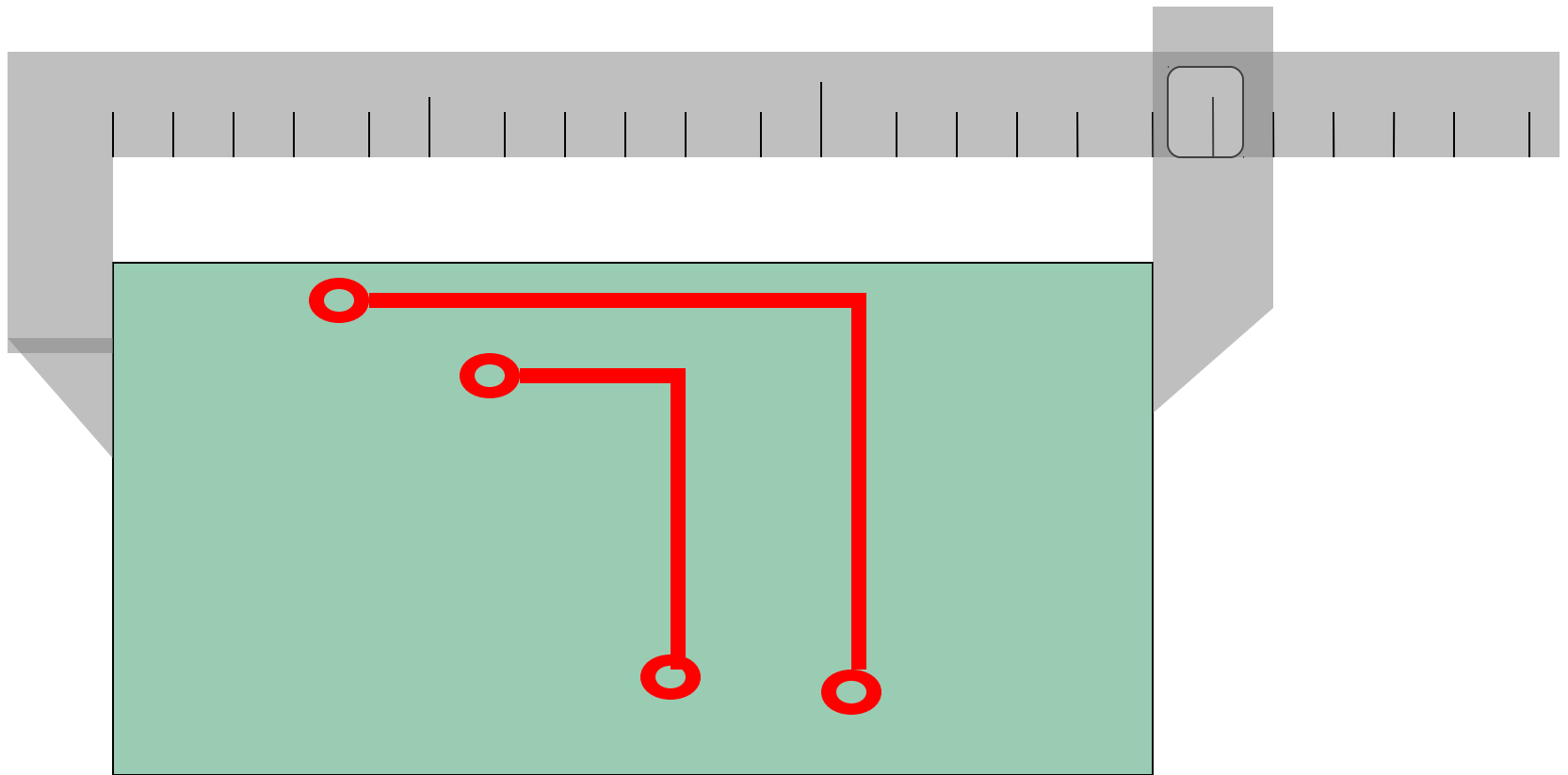
Test électrique

Electrical test



Contrôle

Final Inspection



Expédition *Shipping*



3

Circuits Multicouches Principe de base

Multilayer PCBs *Overview*

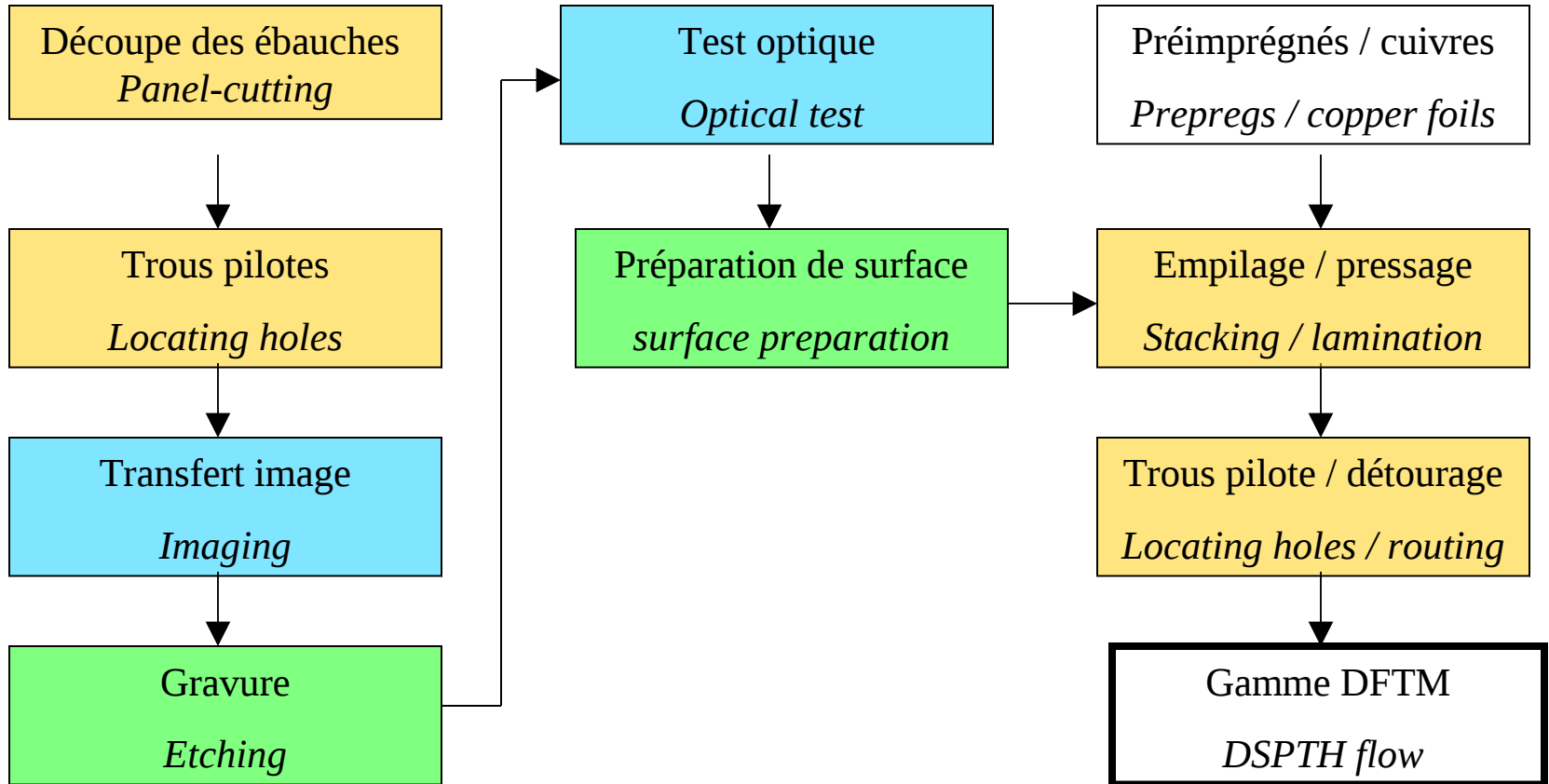
Sommaire

Outline

- Diagramme *Flow chart*
- Poinçonnage *Punching*
- Empilage *Stacking*
- Pressage *Lamination*
- Paramètres *Parameters*

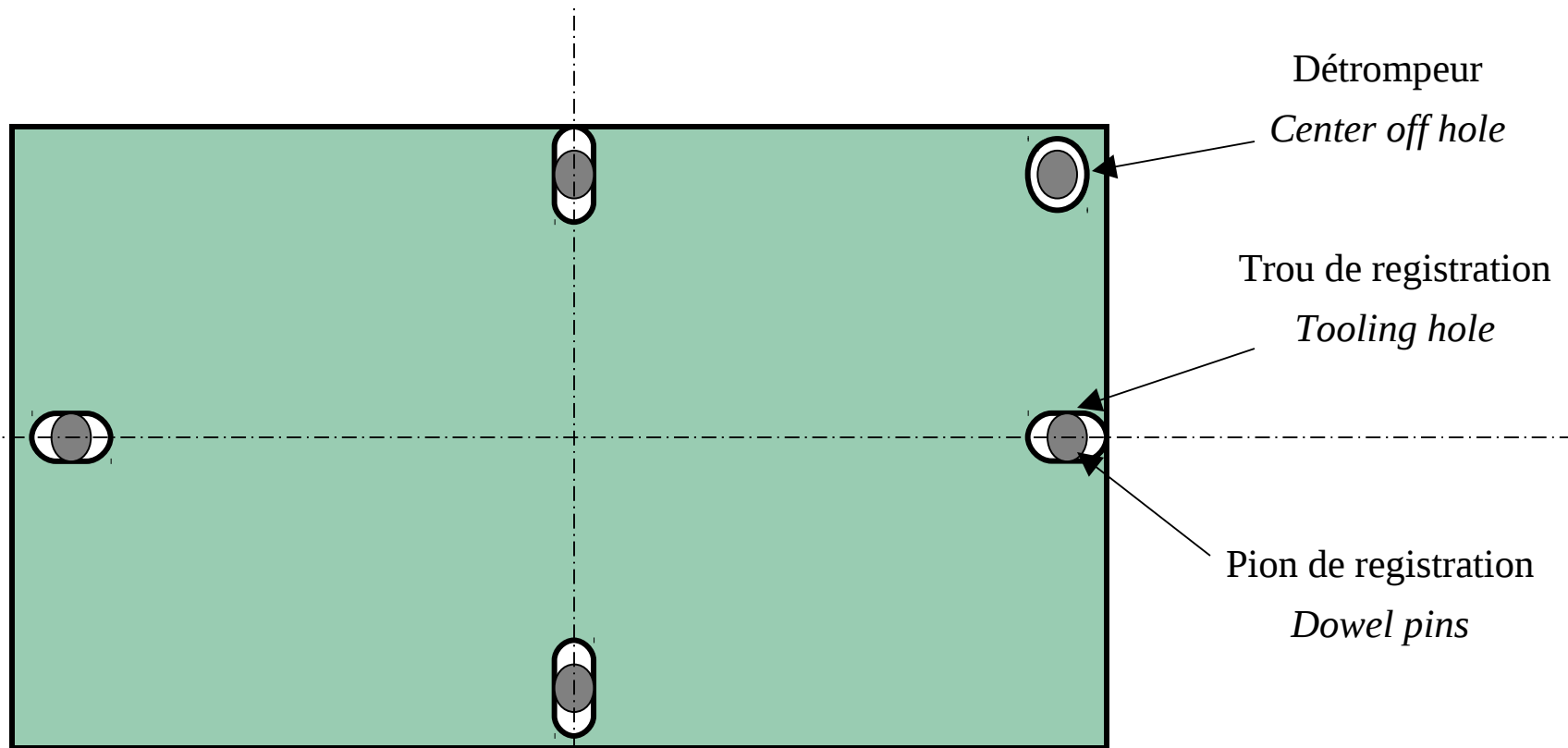
Diagramme

Flow-chart



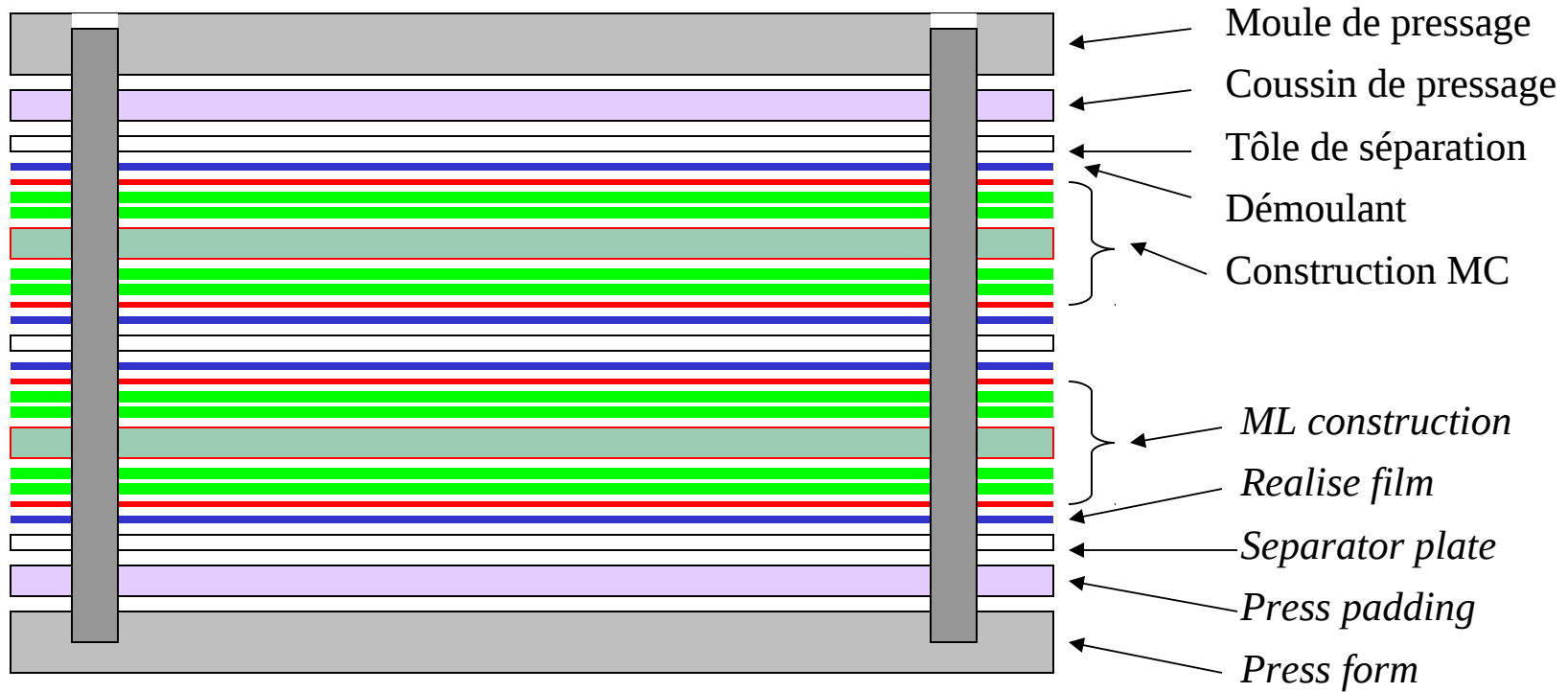
Poinçonnage des trous de registration

Punching of tooling holes

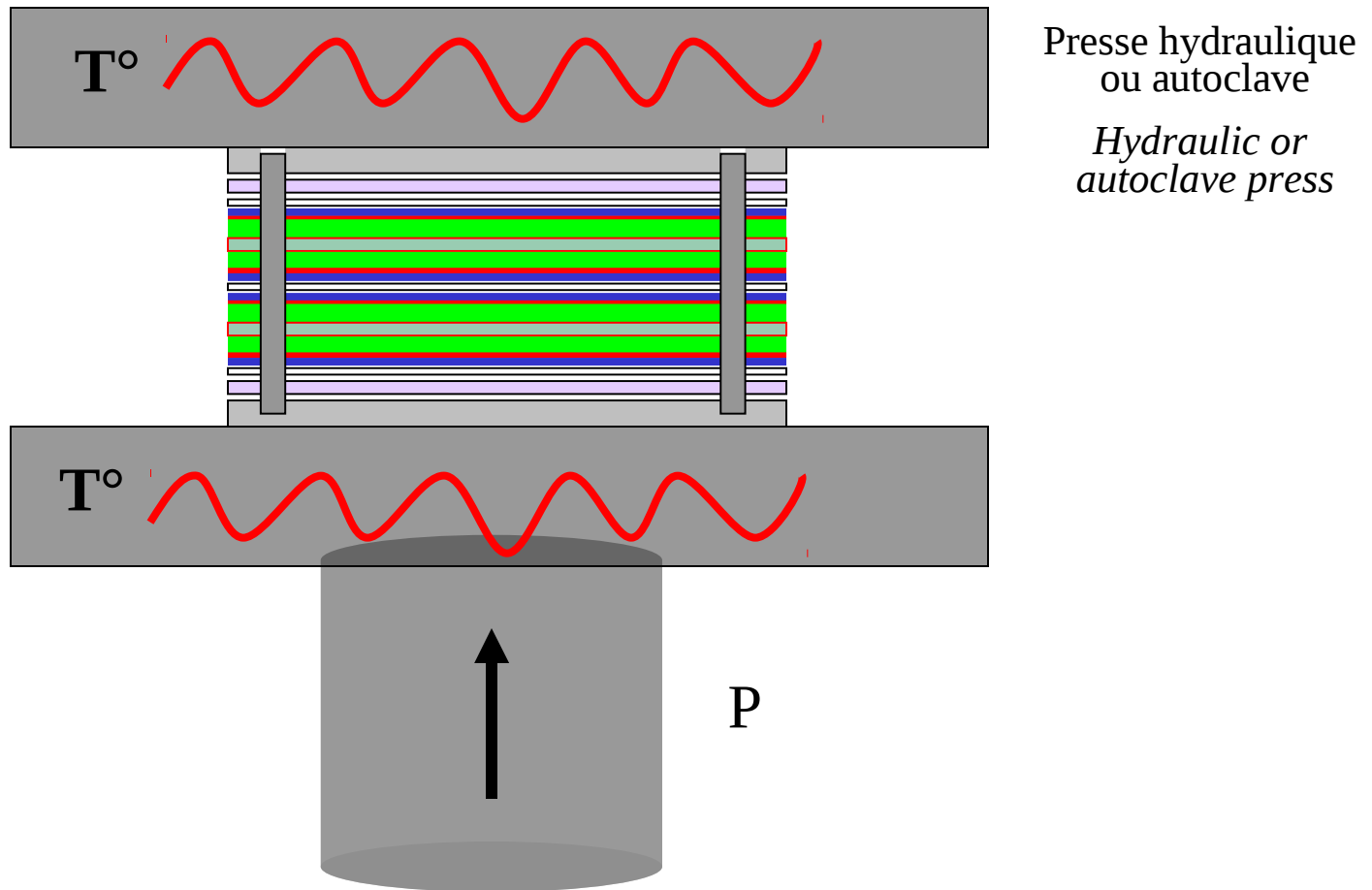


Empilage

Stacking



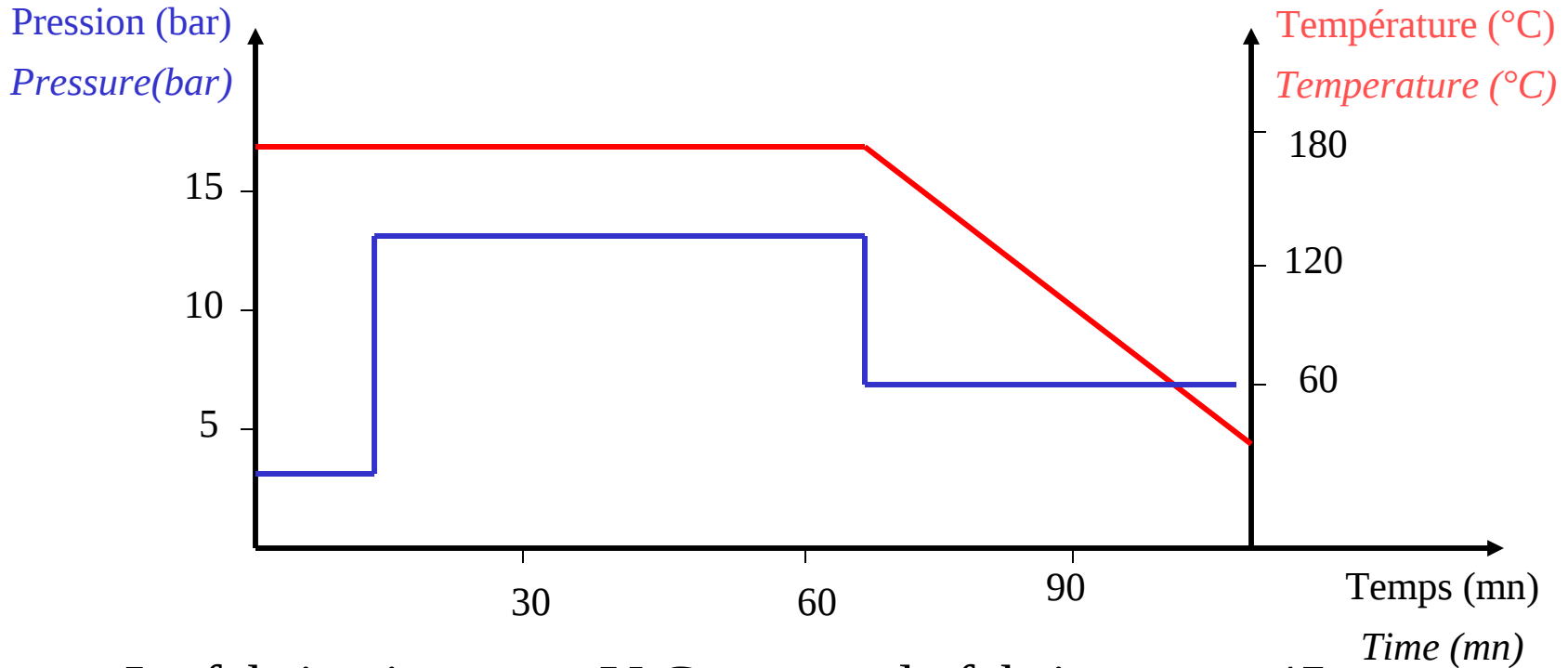
Pressage *Lamination*



Paramètres de pressage

Pressing parameters

Pressage sous vide
Vacuum chamber press



La fabrication
des circuits

V Gammes de fabrica
tion

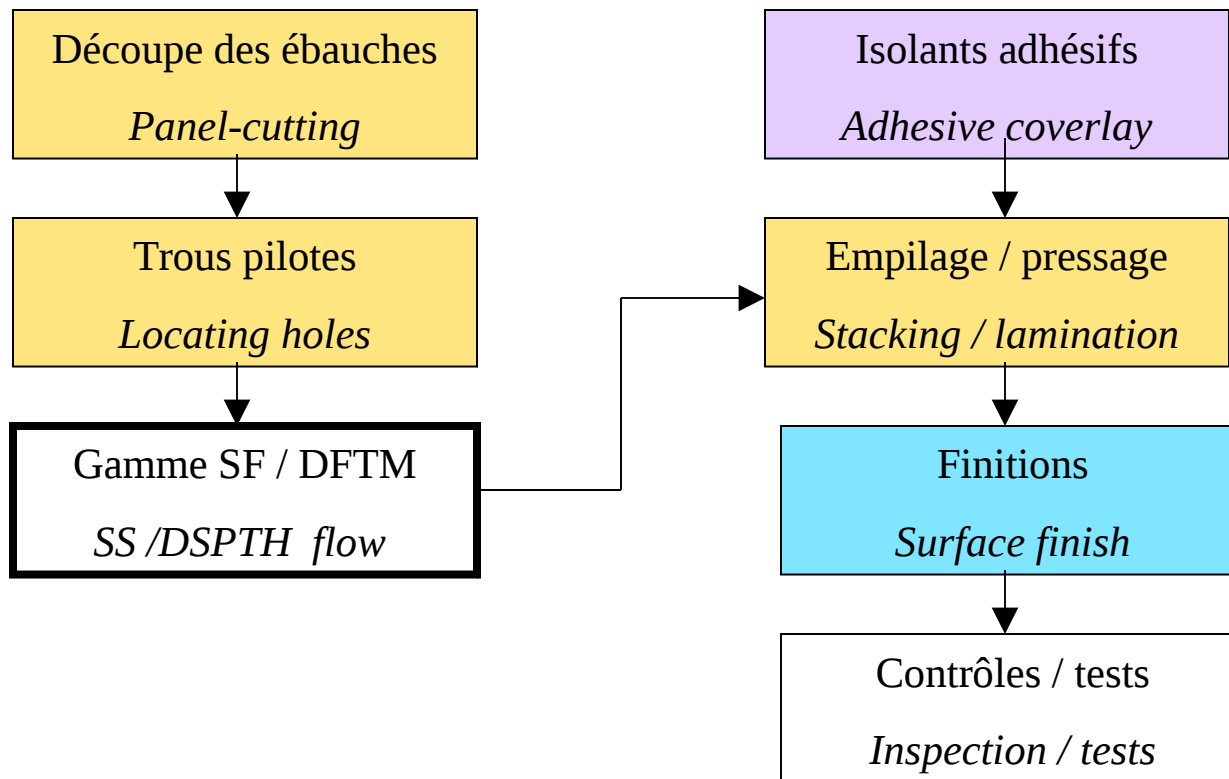
45

4

Circuits Souples
Principe de base

Flexible PCBs
Overview

Diagramme *Flow-chart*



5

Circuits Flexo-rigides Principe de base

Flex-rigid PCBs *Overview*

Diagramme *Flow-chart*

